

1 ABSTRACT OF THE DISCLOSURE

2 The invention includes a number of methods and structures
3 pertaining to semiconductor circuit technology, including: methods of
4 forming DRAM memory cell constructions; methods of forming capacitor
5 constructions; DRAM memory cell constructions; capacitor constructions;
6 and monolithic integrated circuitry. The invention includes a method of
7 forming a capacitor comprising the following steps: a) forming a mass
8 of silicon material over a node location, the mass comprising exposed
9 doped silicon and exposed undoped silicon; b) substantially selectively
10 forming rugged polysilicon from the exposed undoped silicon and not
11 from the exposed doped silicon; and c) forming a capacitor dielectric
12 layer and a complementary capacitor plate proximate the rugged
13 polysilicon and doped silicon. The invention also includes a capacitor
14 comprising: a) a first capacitor plate; b) a second capacitor plate; c)
15 a capacitor dielectric layer intermediate the first and second capacitor
16 plates; and d) at least one of the first and second capacitor plates
17 comprising a surface against the capacitor dielectric layer and wherein
18 said surface comprises both doped rugged polysilicon and doped non-
19 rugged polysilicon.

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